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### CASE STUDY Multicarrier system Linear motor



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Distributed communication and control system on a linear motor with parallel processing in hard real time.

This client required full support and project empowerment from the segment controller board development, Hardware verification, Firmware development, Firmware verification to Mechanical design allowing us to deliver full range of our services and secure top-notch quality. The System is divided into segments: straight and curved. Solution consisted of:

- Segment controller board development
- Hardware verification
- Firmware development
- Firmware verification
- o Mechanical design





### Segment Controller Board Development

System is divided into segments: straight and curved. Each segment consist out of:

- Power board which is responsible for driving the coils (part of a linear motor)
- Coil Controller board which is responsible for controlling the coils and finding the position of a mover by using encoders
- Segment controller which is responsible for maintaining the communication between segments and SERCOS communication at a system level

Segment Controller board is based on Sitara AM6548 SoC from TI which consist out of:

- o 4 x Arm® Cortex® -A53 microprocessor subsystems at up to 1.1 GHz
- o Dual-core Arm® Cortex® -R5F at up to 400 MHz
- Three gigabit Industrial Communication Subsystems (PRU\_ICSSG)
- Up to two 10/100/1000 Ethernet ports per PRU\_ICSSG

128Kx32 LPDDR4 Memory + 256K NOR Flash + 128Kbit NVRAM on board

### Case Study: Multicarrier system Linear motor Hardware Development Cycle



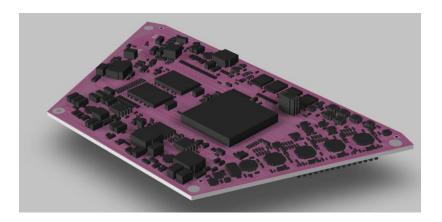
- Requirements capture phase
- Schematic development phase
- o PCB Development phase
- o Signal Integrity Analysis

#### **Used Tools**

- o MS Excel
- Allegro Design Authoring
- Allegro PCB Editor
- Cadence Sigrity

#### **Final Result**

- 12-Layer PCB with controlled impedance for LPDDR4 memory
- 6 power supplies
- 1 LPDDR4 memory chips
- 4 Ethernet PHYs



### Case Study: Multicarrier system Linear motor Hardware Verification Cycle

#### **Requirements driven HW Verification Process**

- o HW Verification requirements phase
- HW Verification Environment Design Phase
- HW Verification Design Phase (schematic + PCB)
- HW Verification Test Development
- HW Verification Test Cycle

#### **Used Tools**

- o MS Excel
- Allegro Design Authoring + Allegro PCB Editor
- National Instruments LabVIEW

#### Used instruments

- o Thermal Chamber
- 4-Channel Digital Storage Oscilloscope
- SMU (Source Measuring Unit)
- Programmable Power Supply

#### Final Result

- Test adapter board with spring loaded test probes
- Pin cushion connection system
- Test Framework running on a PC with LabVIEW
- Thermal chamber for environmental tests controlled directly from LabVIEW app







### Firmware Development

Segment firmware consists of **segment controller applications** (apps for A53 and R5 cores) and **separate firmware for Coil controller board** (based on TI Piccolo MCU family). Synchronization and communication was needed in applications on different boards/cores.

#### Tools/languages:

- C/C++, Python
- TI Eclipse based Code Composer studio IDE
- Octave/Matlab
- Continuous integration / Klocwork / SQUORE

#### **Technical requirements:**

- Hard real time
- Relatively limited memory and CPU resources
- Multithreading and synchronization

#### Hardware:

- Multicore ARM architecture (2xA53 and 2xR5 cores)
- Industrial Ethernet peripheral with accelerator
- Fast custom SPI interface for coil controller communication

#### Activities:

- Complete BSP development (board lib, drivers, bootloader)
- Development of HW validation application and support
- Fast Ethernet communication link development with carrier data exchange protocol
- Application development: Carrier Tracking, File Manager, variable tracing...
- Agile/SCRUM with 3-week sprints
- Unit testing and validation
- Team: 3 FW engineers





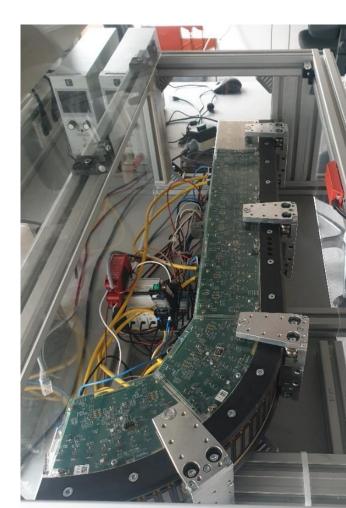
### Firmware Verification

Main achievement: Automation of complete FW testing process

- Complete hardware design (test cabinet), test system built with local supplier
- Decreasing testing time by implementing Jenkins automation
- Test improvements (flexibility, more detailed test reports)
- Development of new tests
- **Drivers Firmware Verification team** consisted of 3 verification engineers.

Technology:

- PLC programming sw (IDE based on CoDeSys, Structure Text, Etest)
- Jenkins 2 (dozens of Freestyle projects) on CI PC
- Python scripting IEC 61131-3
  Code Generator for Object Reassembly
- SVN (for version control)
- TestComplete 14 (GUI automation, Python)
- Autodesk Inventor Professional 2020 and Creo 6 (for mechanical design)
- EPLAN P8 2.8 (for electrical design)
- JIRA and Xray (bug reporting, test creation, planning and execution)





### Mechanical Design

#### **Project Context**

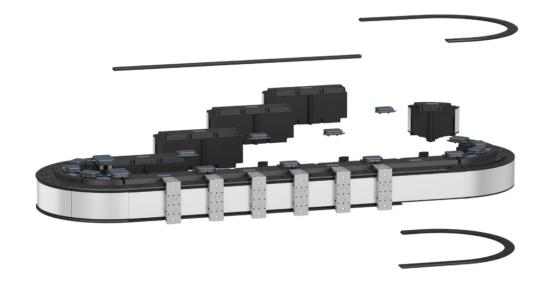
- o Flexible transport system with simplicity in installation and commissioning
- Highly configurable track structure
- High speed workpiece carriers
- Current project phase MP1a (first serial product)

#### Activities

- Mechanical design based on product requirements
- Electronics integration
- Finite Element Analysis (FEA)
- Tolerance analysis
- Design for manufacturing (DFM)
- Prototyping
- o Serial product development

#### **AVISTO Team**

o 2 Mechanical design engineers



## LET'S CONNECT!

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in Connect with us

Where passion leads to excellence



# ABOUT US

### **AVISTO Eastern Europe**

AVISTO Eastern Europe is a service provider that focuses on empowering Industrial automation and Semiconductor projects by offering tailored made solutions in areas of Embedded Systems, Test Automation, Application Software and DevOps.

Established in 2007, AVISTO currently operates three design centers in Serbia and boasts a strong network of experienced engineers empowered by high level of technical adaptability to meet the specific requirements and demands of clients' projects.

As a French company and a member of the Advans Group, which comprises over 1000 engineers, AVISTO can deliver comprehensive product-based development support to clients at the enterprise level. ~\|?568 hD?u (t=b(ls))

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# **THANK YOU**

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